RING MODULATOR/DEMODULATOR TAB101

TENTATIVE DATA

The TAB101 is a monolithic integrated circuit comprising a 4-transistor modulator/demodulator circuit. The circuit, being made on a single crystal, ensures a great similarity in the characteristics of the individual transistors and optimal tracking of their parameters with temperature variation. Consequently, the TAB101 gives better balancing and therefore less carrier leakage than a conventional circuit.

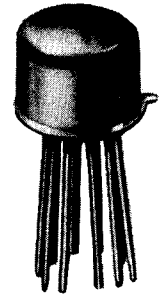
The use of transistors instead of diodes provides a better isolation between input and output circuits.

QUICK REFERENCE DATA

I_{CBO}	Collector-base leakage current $V_{CB}=5.0V$, $T_{amb}=25^{o}C$	<100	nA
$V_{BE1}-V_{BE2}$	Base-emitter voltage difference between transistors Tr1-Tr2 $V_{CB1}=V_{CB2}=5.0V$ $-I_{E1}=-I_{E2}=150\mu A$	<5.0	mV
$V_{BE3}-V_{BE4}$	Base-emitter voltage difference between transistors Tr3-Tr4 $V_{CB3}=V_{CB4}=5.0V$ $-I_{E3}=-I_{E4}=150\mu A$	<5.0	mV
$h_{FB1}-h_{FB2}$	Common base current amplification difference between transistors Tr1-Tr2 $V_{CB1}=V_{CB2}=5.0V$, $-I_{E1}=-I_{E2}=150\mu A$	<0.008	
$h_{FB3}-h_{FB4}$	Common base current amplification difference between transistors Tr3-Tr4 $V_{CB3}=V_{CB4}=5.0V$, $-I_{E3}=-I_{E4}=150\mu A$	<0.008	

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-74
B.S. 3934 SO-44/SB10-1



RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical (each transistor)

V_{CBO} max.	Collector-base voltage	10	V
V_{EBO} max.	Emitter-base voltage	5.0	V
V_{CS} max.	Collector-substrate voltage	12	V
I_C max.	Collector current	10	mA

Power (4 transistors)

P_{tot} max.	Total power dissipation	100	mW

Temperature

T_{stg} min.	-35	^oC
T_{stg} max.	+125	^oC
T_{amb} min. (operating)	-25	^oC
T_{amb} max. (operating)	+100	^oC

CHARACTERISTICS (Each transistor, $T_{amb} = 25^oC$)

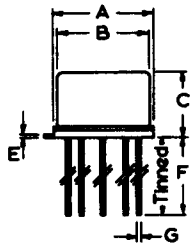
Static characteristics		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 10\mu A$, $I_E = 0$	10	-	-	V
$V_{CE(sust)}$	Collector-emitter sustaining voltage $I_C = 10\mu A$, $I_B = 0$	9.0	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 200\mu A$, $I_C = 0$	5.0	-	-	V
$V_{(BR)CS}$	Collector-substrate breakdown voltage $-I_S = 10\mu A$	12	-	-	V
I_{CBO}	Collector-base leakage current $V_{CB} = 5.0V$, $I_E = 0$	-	5.0	100	nA
I_{EBO}	Emitter-base leakage current $V_{EB} = 1.0V$, $I_C = 0$	-	5.0	100	nA
I_{CS}	Collector-substrate leakage current $V_{CS} = 9.5V$	-	5.0	100	nA

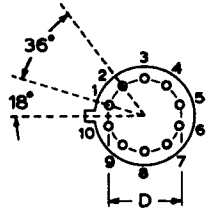
CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
Static characteristics					
h_{FE}	Large signal forward current transfer ratio $I_C = 150\mu A$, $V_{CE} = 5.0V$	20	75	-	
Dynamic characteristics					
f_T	Transition frequency $-I_E = 150\mu A$, $V_{CB} = 5.0V$, $f = 35MHz$	-	100	-	MHz
N	Spot noise factor $f = 1.0kHz$, Bandwidth = 200Hz, $R_{source} = 1.8k\Omega$, $-I_E = 150\mu A$, $V_{CB} = 5V$	-	-	10	dB
Matching of transistors					
$V_{BE1}-V_{BE2}$	Base-emitter voltage difference between transistors Tr1-Tr2 $V_{CB1} = V_{CB2} = 5.0V$, $-I_{E1} = -I_{E2} = 150\mu A$	-	2.0	5.0	mV
$V_{BE3}-V_{BE4}$	Base-emitter voltage difference between transistors Tr3-Tr4 $V_{CB3} = V_{CB4} = 5.0V$, $-I_{E3} = -I_{E4} = 150\mu A$	-	2.0	5.0	mV
$h_{FB1}-h_{FB2}$	Common base current amplification difference between transistors Tr1-Tr2 $V_{CB1} = V_{CB2} = 5.0V$, $-I_{E1} = -I_{E2} = 150\mu A$	-	0.002	0.008	
$h_{FB3}-h_{FB4}$	Common base current amplification difference between transistors Tr3-Tr4 $V_{CB3} = V_{CB4} = 5.0V$, $-I_{E3} = -I_{E4} = 150\mu A$	-	0.002	0.008	
Operating conditions (see typical circuit on page 5)					
P_{out}/P_{in}	Conversion gain $f_c = 34kHz$, $f_a = 1kHz$, $V_{in} = 0.4V$	-	-0.75	-	dB
P_{oc}	Carrier leakage power $f_c = 34kHz$	-	3.0	-	nW

OUTLINE AND DIMENSIONS

Pins	
1.	Substrate
2.	Collector Tr1 and Tr4
3.	Base Tr1
4.	Emitter Tr1 and Tr3
5.	Base Tr3 and Tr4
6.	Collector Tr2 and Tr3
7.	Base Tr2
8.	Emitter Tr2 and Tr4
9.	N.C.
10.	N.C.

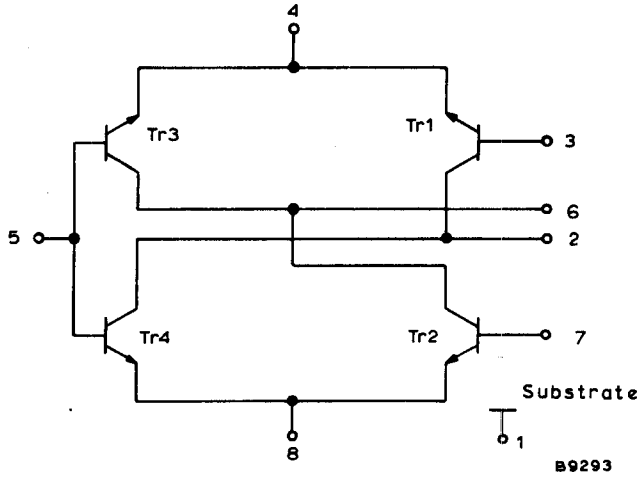




	Millimetres		
	Min.	Nom.	Max.
A	8.64	8.90	9.40
B	7.75	8.15	8.50
C	-	-	5.33
D	-	5.08	-
E	-	0.40	-
F	12.7	-	-
G	-	0.43	-

Pin 1 connected to envelope and substrate
10 pins on 360° spaced equally

CIRCUIT DIAGRAM



TYPICAL CIRCUIT